Register No : _____

THE KAVERY ENGINEERING COLLEGE

(An Autonomous Institution)

B.E/B.TECH DEGREE END SEMESTER THEORY EXAMINATIONS, NOV/DEC 2025

Third Semester

Electrical and Electronics Engineering

EE3302 – Digital Logic Circuits

Regulations – 2021

Duration : 3 Hrs *Maximum : 100 Marks*

*PART – A (ANSWER ALL QUESTIONS) (Marks 10*2=20)*

Q.No	*Questions*	*BTL*	*CO*	*Marks*
1.	Convert the number (255)10 to its binary equivalent.	L2	1	2
2.	Recall the advantages and disadvantages of TTL.	L1	1	2
3.	Draw 8*1 multiplexer using only 4*1 multiplexer.	L1	2	2
4.	Label the circuit of half subtractor and write its truth table.	L1	2	2
5.	Compare between combinational and sequential circuits.	L2	3	2
6.	Infer the rules for state assignment.	L2	3	2
7.	Sketch the general architecture of CPLD.	L1	4	2
8.	How the hazards in combinational circuits can be removed?	L1	4	2
9.	When can RTL be used to represent digital systems?	L1	5	2
10.	Write VHDL code for half adder in data flow model.	L1	5	2

*PART – B (ANSWER ALL QUESTIONS) (Marks 5*16 = 80)*

Q.No			*Questions*	*BLT*	*CO*	*Marks*
11.	a	i	Encode the binary word 1011 into seven bit even parity hamming code.	L2	1	8
		ii	How can the expression Y=(A+B).C can be implemented using NAND gates?	L2	1	8
			Or			
	b	i	Elucidate the operation of TTL NAND gate with relevant circuit diagrams.	L2	1	8
		ii	Draw the MOS logic circuit for NOT gate and explain its operation.	L2	1	8
12.	a		Use Quine McCluskey principle to simplify the expression f=∑m(1,2,3,5,6,7,8,9,12,13,15) and implement the same using logic gates.	L3	2	16
			Or			
	b		Develop a 4 bit gray to binary code converter using K-map.	L3	2	16
13.	a		With relevant diagrams, explain the working of bidirectional shift registers.	L5	3	16
			Or			
	b		Determine the logic diagram of MOD 12 synchronous counter using JK flip flops with neat diagram.	L5	3	16

14.	a	Simplify the full adder using PAL and ROM.	L4	4	16
		Or			
	b	Contrast in detail the various types of hazards in sequential circuit design and the methods to eliminate them with relevant examples.	L4	4	16
15.	a	Build the VHDL coding for adders to realize its structural modeling.	L3	5	16
		Or			
	b	Apply in detail the RTL design procedure with relevant sketches.	L3	5	16